In the Claims

Please replace all prior versions, and listings, of claims in the application with the following listing of claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing:

Listing of Claims

1. (Currently amended) A method of verifying a digital hardware design simulated in a hardware design language (HDL), including the steps of:

defining at least one state to be verified, the at least one state including a set of signal values, each signal value ~~for each~~ corresponding to a respective one of a plurality of components within the hardware design;

applying a test to the hardware design;

generating traces of internal signals within the hardware design during the test, each trace including signal data, ~~and~~ time data and ~~including at least the defined for~~ internal ~~signals~~ signal values associated with ~~a respective one of~~ the plurality of components; and

processing the traces to ascertain whether the plurality of components simultaneously had the signal values defined for ~~associated with~~ the at least one state, thereby to ascertain whether the at least one state was achieved.

2. (Currently Amended) A method according to claim 1, wherein more than one state is defined, each state including a set of signal values, each signal value ~~for each~~ corresponding to a respective one of a plurality components of the hardware design, the traces being processed to ascertain, for each state, whether the corresponding plurality of components simultaneously had the signal values defined for ~~associated with~~ the state, thereby to ascertain whether each of the states was achieved.

3. (Original) A method according to claim 2, wherein the processing step includes ascertaining whether a predetermined sequence of states was achieved.

4. (Original) A method according to claim 3, wherein the processing step includes ascertaining whether a given state in a sequence was achieved within a predetermined time period after an earlier state in the sequence.

5. (Currently Amended) A method according to claim 1, wherein the traces are pre-processed prior to the processing step, such that, for at least each of the components for which a signal value is defined within the at least one state~~each of the states~~, the trace associated with the component includes a signal value ~~for the respective signals associated with those components exists~~ for each time for which the traces are to be processed.

6. (Original) A method according to claim 1, wherein one or more of the signal values are values of a field associated with the corresponding component.

7. (New) A method of verifying a digital hardware design simulated in a hardware design language (HDL), including the steps of:

defining at least one state to be verified, the at least one state including a set of signal values, each signal value corresponding to a respective one of a plurality of components within the hardware design;

applying a test to the hardware design;

generating traces of internal signals within the hardware design during the test, each trace including signal data, time data and internal signal values associated with a respective one of the plurality of components;

pre-processing the traces such that, for at least each of the components for which a signal value is defined within the at least one state, a trace associated with the component includes a signal value for each time for which the traces are to be processed; and

processing the traces to ascertain whether the plurality of components simultaneously had the signal values defined for the at least one state, thereby to ascertain whether the at least one state was achieved.

8. (New) A method according to claim 7, wherein more than one state is defined, each state including a set of signal values, each signal value corresponding to a respective one of a plurality components of the hardware design, the traces being processed to ascertain, for each state, whether the corresponding plurality of components simultaneously had the signal values defined for the state, thereby to ascertain whether each of the states was achieved.

9. (New) A method according to claim 8, wherein the processing step includes ascertaining whether a predetermined sequence of states was achieved.

10. (New) A method according to claim 9, wherein the processing step includes ascertaining whether a given state in a sequence was achieved within a predetermined time period after an earlier state in the sequence.

11. (New) A method according to claim 7, wherein one or more of the signal values are values of a field associated with the corresponding component.

12. (New) A method of verifying a digital hardware design simulated in a hardware design language, the design including a plurality of components, wherein at least one state is defined by a set of signal values, each signal value corresponding to a respective one of the plurality of components, the method comprising:

generating traces of internal signals within the hardware design during application of a test to the hardware design, each trace including signal values associated with a respective one of the plurality of components; and

determining whether the at least one state was achieved, including comparing signal values within the traces to the set of signal values defined for the at least one state.

13. (New) The method of claim 12, wherein the determining of whether the at least one state was achieved includes determining whether, at a given time during the test, each signal value of the set of signal values is equal to a corresponding signal value included within one of the traces.

14. (New) The method of claim 12, wherein a plurality of states are defined, and wherein the step of determining includes determining whether each of the plurality of states was achieved.

15. (New) The method of claim 14, further comprising:
determining whether a particular sequence of the plurality of states was achieved.

16. (New) The method of claim 15, further comprising:
determining whether one of the states in the sequence was achieved within a particular time period after another state in the sequence was achieved.

17. (New) The method of claim 12, further comprising:
prior to determining whether the at least one state was achieved, pre-processing the traces such that, for at least each of the components for which a signal value is defined within the at least one state, the trace associated with the component includes a signal value for each time during the test for which it is determined whether the at least one state was achieved.

18. (New) The method of claim 12, wherein, for each of one or more of the signal values defined for the at least one state, the signal value represents a value of a field associated with the respective one of the plurality of components corresponding to the signal value, and
wherein the generating of traces of internal signals includes generating signal values of the fields.

19. (New) The method of claim 12, wherein the generating of traces comprises including time data in each trace indicative of one or more times at which the internal signal values in the trace were detected.